Pramod Kumar Bharti
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ACADEMIC DETAILS

Degree	University/Board	Institute	Year	CPI/%
Ph.D	IIT Gandhinagar	IIT Gandhinagar	2016-present	7.45
Post Graduation	IIT Indore	IIT Indore	2014-2016	8.88
UnderGraduation	NIT Trichy	NIT Trichy	2009-2013	7.14

FIELDS OF INTEREST

- Vlsi Design, CMOS Analog IC Design.

TECHNICAL SKILLS

- **Languages**: C, C++, Verilog HDL, Skill scripting,Ocean Scripting, Python.
- **Tools/Softwares**: Cadence Virtuoso, Vivado, Xilinx ISE, MATLAB, LaTeX.

PUBLICATIONS

- **Bharti, Pramod Kumar**, Neelam Surana, and Joycee Mekie. "Power and Area Efficient Approximate Heterogeneous 8T SRAM for Multimedia Applications." 2019 32nd International Conference on VLSI Design and 2019 18th International Conference on Embedded Systems (VLSID). IEEE, 2019 **(nominated for best paper award)**.
- **Bharti, Pramod Kumar**, Neelam Surana, and Joycee Mekie. "Hetro8T: Power and Area Efficient Approximate Heterogeneous 8T SRAM for H.264 Video Decoder." IET Computers Digital Techniques,no. 11, pp. N 1751-8644, June. 2019 **(Journal)**.
- **Bharti, Pramod Kumar**, Neelam Surana, and Joycee Mekie. "Mixed Vt 8T SRAM for H.264 Video Processor." IEEE Transactions on Very Large Scale Integration (TVLSI) Systems , october. 2019 **(Journal- unverreview)**.
- **Collaboration with Intel**. "Compute in memory 6T SRAM for variety of workloads." IEEE Transactions on Very Large Scale Integration (TVLSI) Systems. **(Journal- to be submitted)**.

MAJOR PROJECTS

- **PhD. Thesis** *Prof: Joycee Mekie*
  Approximate memory design for H.264 Video CoDec (Compression and Decompression)
  - Exponential growth in internet availability and low-cost smart-phones have led to huge increase in viewership of video, which requires an energy-efficient compression/ decompression circuit.
  - since 60 % of the total area is consumed in the SRAM used in H.264 video CoDec alone, so we have design power and area efficient SRAM memory for H.264 CoDec.
  - A 1 Kb heterogeneous 8T SRAM architecture is proposed for H.264 video decoder, which gives better PSNR even at low power and area budget.
  - A 1 Kb memory of mixed Vt based 8T SRAM architecture is proposed for H.264 video decoder, which gives zero error even at minimum SRAM cell size. The design is suitable for all the videos starting from QCIF to ultra HD and so on.
  - Skill scripting is used to design 1 Kb proposed SRAM memory. Ocean scripting is used to automate the simulations which are done in Cadence Virtuoso.
  - H.264 CoDec is designed using MATLAB. A 4:2:0 YCbCr video format is used during compression/ decompression.

- **Compute in memory 6T SRAM for variety of workloads** *In Collaboration with Intel*
  - we present a write disturb free split 6T bitcell-based compute in memory subarray with variable multi-bit precision for input operands and outputs.
  - The split wordlines of the 6T cell enables sign segregation, thus enabling arbitrary sign/magnitude multiply and accumulate (MAC) operations.
- **Front End Design of Various Adders and Multiplier in Verilog using XILINX-ISE** : *Prof:Nithin George*
  - A ripple carry adder, and a carry-save adder are designed and simulated in Verilog using XILINX-ISE suite.
  - A booth multiplier and Wallace Tree Multiplier are designed and simulated in Verilog using XILINX-ISE suite.
- **Front End Design of 32 bit Floating Point Arithmetic Unit Implementation in Verilog using XILINX-ISE**: *Prof:Joycee Mekie*
  - A IEEE-754 format based 32 bit floating point arithmetic unit is designed.
  - The floating-point arithmetic unit performs various operations like addition, subtraction and multiplication was designed in Verilog. The design is also synthesized using XILINX-ISE suite.

CONFERENCES & WORKSHOPS

- **Conference: VLSI Design 2018** (Delhi)
  Presented my paper on power and area efficient SRAM design for multimedia applications such as H.264 Encoder- Decoder (CoDec).
- **Conference: VLSI Design 2018** (Pune)
  Attended 4 days conference in which theme of the conference is green energy.
- **Conference: VLSI Design and Test (VDAT) 2019** (Indore)
  Attended 3 days conference in Indore.
- **Attended two days workshop on Linear Integrated Circuit and System approach by Texas Instruments** (September-2016):
  The workshop intended to gain a better hands-on analog system lab development kit.

ACHIEVEMENTS

- Recipient of Silver -72 scholarship.
- Secured 4^{th} Rank in Bihar Combined Entrance Competitive Examination (BCECE) with a percentile of 99.9.
- Secured 4112 Rank in All India Engineering Entrance Examination (AIEEE) with a percentile of 99.9.
- Secured 1714 Rank in Graduate Aptitude Test (GATE) with a percentile of 99.4.

POSITION OF RESPONSIBILITIES

- Worked as a Teaching Assistant in the Electrical and Electronics laboratory.
- Worked as a Teaching Assistant in the Analog Design laboratory.